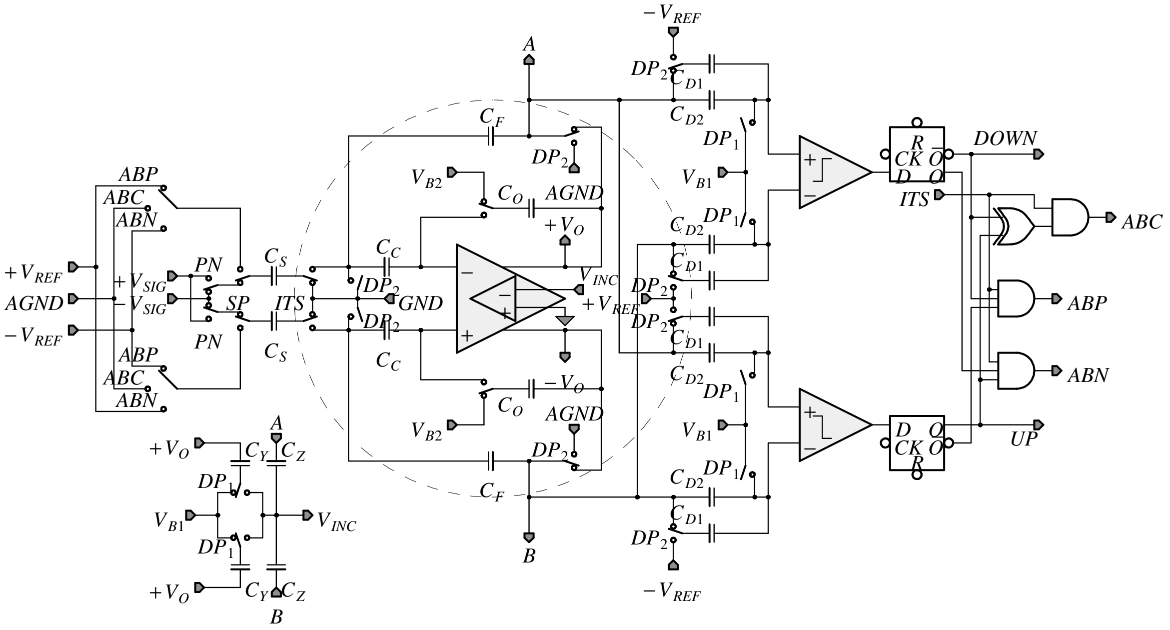
The following slide shows the complete schematics of the fully-differential RIC. The operation includes a correlated-double-sampling phase that occurs once every 256 clock periods, also called the *spreading ratio*. This reset phase is controlled by clocks DP_1 and DP_2 in which the integrator is initialized by totally removing the charge from C_F and storing the low-frequency noise of the op amp in C_C. At the same time the comparison thresholds are set.



The faster clocks are PN, ITS and SP. The sampling capacitor C_S performs the delayed subtraction of a sample of the input signal $\pm V_{SIG}$ and a choice of $-V_{REF}$, $AGND$ or $+V_{REF}$ according to the operations performed by the logic partially depicted operating on past results of the comparisons. The synchronous comparators are reset at this fast rates, thus performing one comparison for every fast clock cycle. The dynamic common-mode feedback arrangement operates synchronously with the reset time slot and its configuration is equivalent to that in the differential feedback path.